Tentative Product Specification

Module name: P0340WQLB-T

Issue date: 2008/03/19

Version: 1.1

Customer		
Approved by Customer		
Approved by CMEL		
PD Division	**ENG Division**	**QA Dept**

Note:

1. The information contained herein may be change without prior notice. It is therefore advisable to contact CHI MEI EL Corp. before designed your product based on this specification.

Reversion History

Version	Date	Page	Description
Ver.1.0	2008/02/29	All	Tentative specification was first issued
Ver.1.1	2008/03/19	18	Change External Dimension

1. Purpose:

This documentation defines general product specification for OLED module supplied by CMEL. The information described in this technical specification is tentative. Please Contact CMEL's representative while your product is modified.

2. General Description:

- Driving Mode: Active Matrix
- Color Mode: Full Color (16M color)
- Driver IC: HX5116, COG Assembly
- Interface:
  8bit serial RGB and 24bit parallel RGB interface
- Application: Portable DVD, PMP, GPS, Photo Frame etc.

3. Mechanical Data:

No.	Items	Specification	Unit
1	**Diagonal Size**	3.4	Inch
2	**Resolution**	480 RGB x 272	
3	**Pixel Pitch**	H: 156 V: 156	um
4	**Active Area**	74.88 x 42.43	mm
5	**Outline Area**	82.8 x 54.3	mm
6	**Thickness**	2.8	mm
7	**Weight**	TBD	g

4. Maximum ratings:

Symbol	Parameter	Value	Unit
VCC	Logic Supply Voltage	-0.3 to +3.6	V
VCI	Analog Supply Voltage	-0.3 to +3.6	V
TA	Operating Temperature	-20 to +60	℃
Tstg	Storage Temperature	-40 to +85	℃

Table 7.1 Maximum ratings

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section. Unused outputs must be left open.

5. Electrical Characteristic:

5.1 DC Characteristic

DC Characteristics

(Unless otherwise specified, Voltage Referenced to VSS = 0V, VCC = 1.5 to 3.6V, T_A = -20 to 70C)

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
System power supply pins of the logic block	VCC	-	1.5	-	3.6	V
Booster Reference Supply Voltage Range	VCI	-	3.0	-	3.6	V
DDVDH Output Voltage 1	DDVDH	Set CP1X=0	4.9	5.1	5.3	V
DDVDH Output Voltage 2	DDVDH	Set CP1X=1	5.8	6.0	6.2	V
VGAM1OUT Output Voltage 1	VGAM1OUT	Set CP1X=0	4.7	4.8	4.9	V
VGAM1OUT Output Voltage 2	VGAM1OUT	Set CP1X=1	5.7	5.8	5.9	V
Gate driver High Output Voltage	VGH	-	+3	-	+8	V
Gate driver Low Output Voltage	VGL	-	-8	-	-3	V
OLED Diode Refer Voltage	ARREF	-	-8	-	+8	V
Logic High Output Voltage	VOH	Iout=-400µA	0.8 * VCC	-	VCC	V
Logic Low Output Voltage	VOL	Iout=400µA	0	-	0.2 * VCC	V
Logic High Input voltage	VIH	-	0.8 * VCC	-	VCC	V
Logic Low Input voltage	VIL		0	-	0.2 * VCC	V
Logic Input Current	IIL/IIH	No pull up or pull low	-1	-	1	µA
Pull high resistance	RH	Pull up pins	600	900	1200	KΩ
Pull low resistance	RL	Pull low pins	600	900	1200	KΩ
High Output Current	IOH	S1~S107, Vo=4.9V vs. 4V	50	-	-	µA
Low Output Current	IOL	S1~S107, Vo=0.1V vs. 1V	-	-	-50	µA
Output leakage Current	IOZ	-	-1	-	1	µA
Output voltage offset	VOS	S1~S107, Vo=0.1V~DDVDH-0.1V		±10		mV
Output voltage deviation	VOD	S1~S107, Vo=0.1V~DDVDH-0.1V		±10		mV
Analog standby current	ISTB	VCI=3.0V, Stand by mode		-	10	uA
Analog operating current	IVCI	VCI=3.0V, S1~S160 no load		TBD		mV
Analog operating current	IVCI	VCI=3.0V, S1~S160 no load		TBD		mV
Logic Pins Input Capacitance	CIN	-	-	5	7.5	pF

5.2 AC Characteristic

5.2.1 AC Electrical Characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
HSYNC setup time	T_{hst}	10	-	-	ns
HSYNC hold time	T_{hhd}	10	-	-	ns
VSYNC setup time	T_{vst}	10	-	-	ns
VSYNC hold time	T_{vhd}	10	-	-	ns
Data setup time	T_{dsu}	10	-	-	ns
Data hold time	T_{dhd}	10	-	-	ns
DE setup time	T_{esu}	10	-	-	ns
VSYNC falling to HSYNC falling time on odd field @ RGB mode	T_{HV_O}	-4	0	+4	T_{CPH}
VSYNC falling to HSYNC falling time on even field @ RGB mode	T_{HV_E}	0.4	0.5	0.6	T_H
Source output settling time	T_{ST}	-	3	-	µs
Source output loading R	R_{SL}	-	25	-	K ohm
Source output loading C	C_{SL}	-	16	-	pF
Gate signals settling time (90%)	T_{GL}	-	0.5	-	µs
Gate signals loading R	R_{GL}	-	5.6	-	K ohm
Gate signals loading C	C_{GL}	-	30	-	pF
SW signals settling time (90%)	T_{SW}	-	0.6	-	µs
SW signals loading R	R_{SW}	-	1.4	-	K ohm
SW signals loading C	C_{SW}	-	85.5	-	pF

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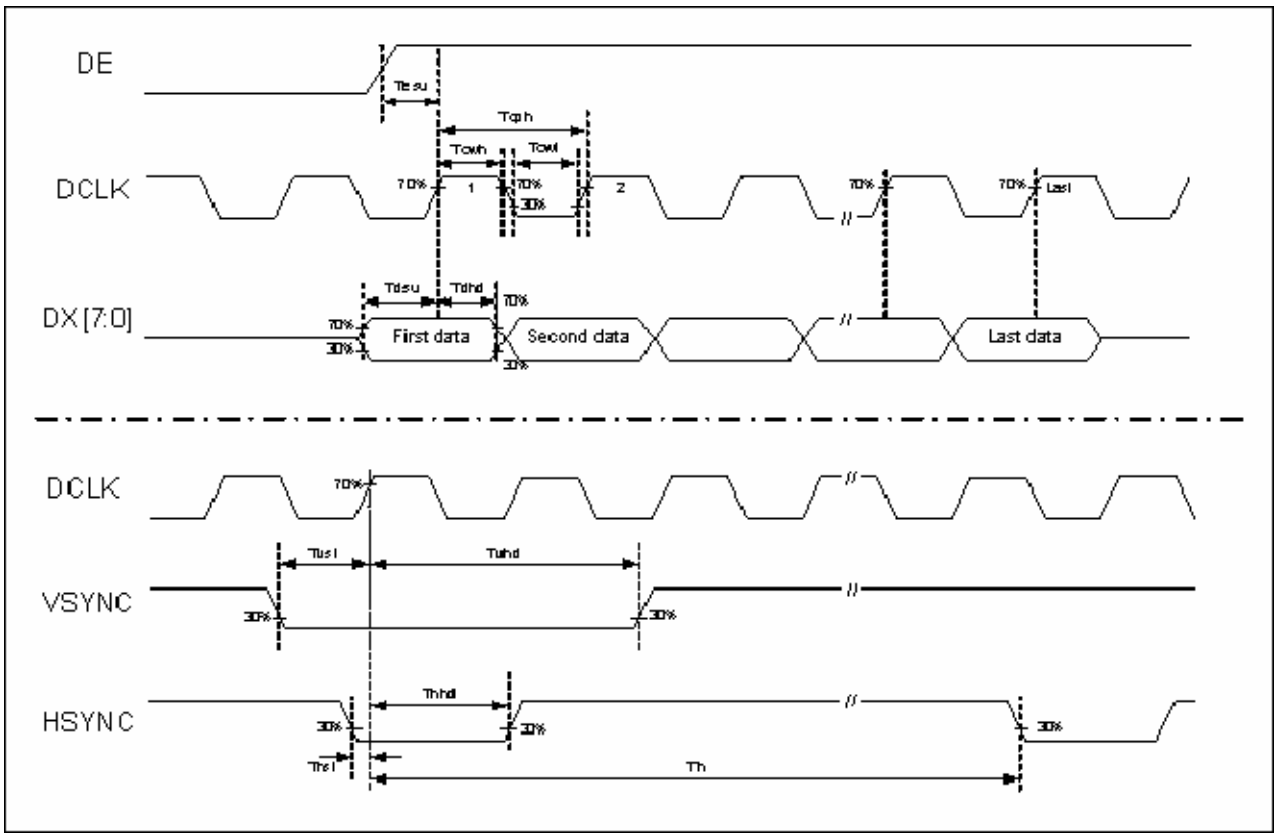
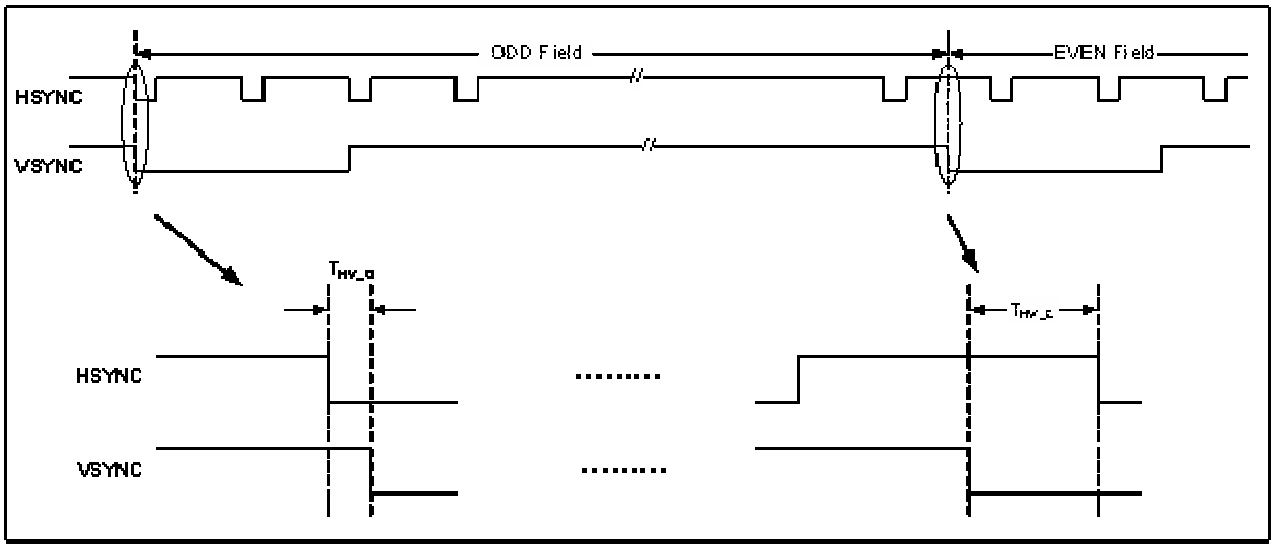


Clock and Data input waveforms



Define the HSYNC to VSYNC timing for RGB mode

5.2.2 480RGB X 272 serial RGB interface

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	F_{CPH}	33.3	-	-	MHz
DCLK period	T_{CPH}	-	-	30	ns
DCLK pulse duty	T_{CWH}	40	50	60	%
HSYNC period	T_H	-	1836	-	T_{CPH}
HSYNC pulse width	T_{WH}	5	90	-	T_{CPH}
HSYNC-first horizontal data time	T_{HBP}	274	306	337	T_{CPH}
DE pulse width	T_{EP}	-	1440	-	T_{CPH}
VSYNC pulse width	T_{WV}	1	3	5	T_H
VSYNC-1st Data input (DE) time	T_{VBP}	4	20	35	T_H
VSYNC period	T_V	302	-	-	T_H

5.2.2 480RGB X 272 parallel RGB interface

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	F_{CPH}	11.1	-	-	MHz
DCLK period	T_{CPH}	-	-	90	ns
DCLK pulse duty	T_{CWH}	40	50	60	%
HSYNC period	T_H	-	612	-	T_{CPH}
HSYNC pulse width	T_{WH}	5	30	-	T_{CPH}
HSYNC-first horizontal data time	T_{HBP}	70	102	133	T_{CPH}
DE pulse width	T_{EP}	-	480	-	T_{CPH}
VSYNC pulse width	T_{WV}	1	3	5	T_H
VSYNC-1st Data input (DE) time	T_{VBP}	4	20	35	T_H
VSYNC period	T_V	302	-	-	T_H

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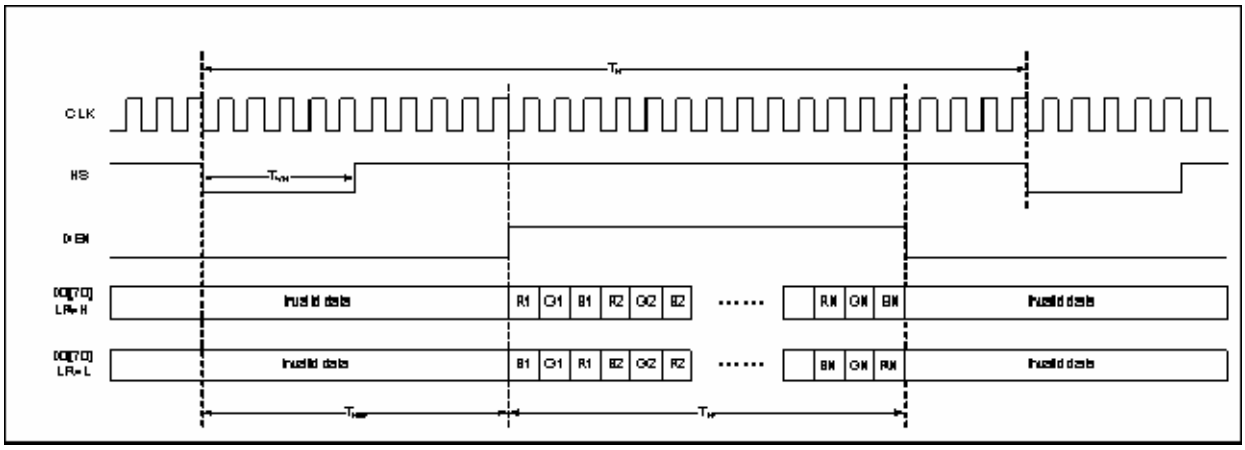
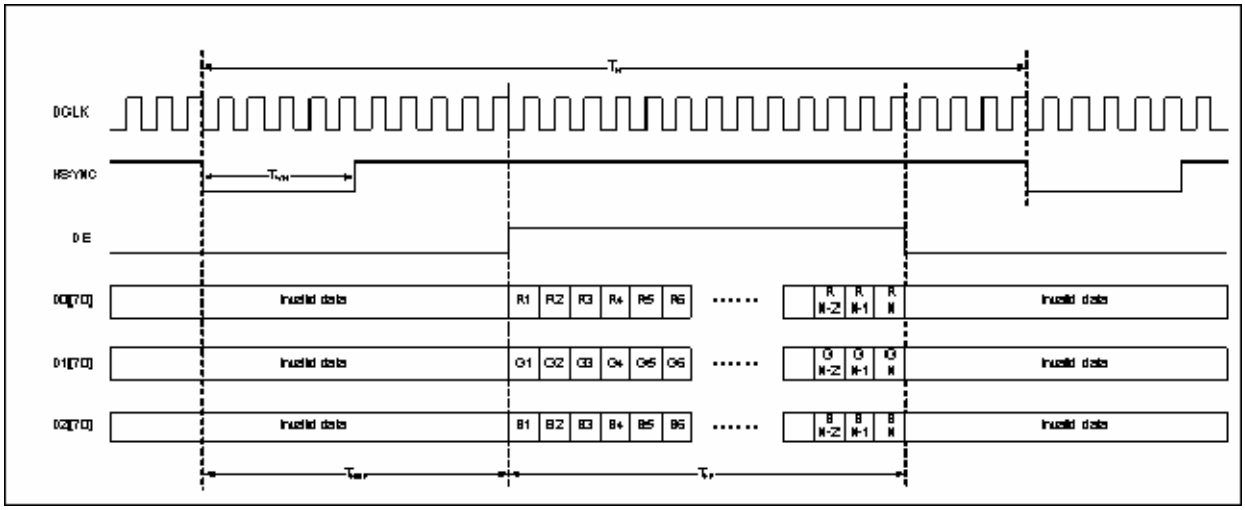
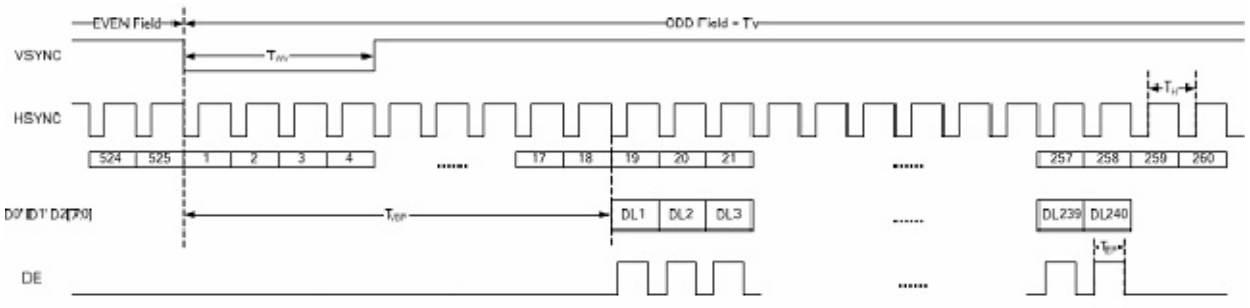


Serial RGB Horizontal Data Format



Parallel RGB Horizontal Data Format



Digital RGB Vertical Data Format

6. Electro-Optical Characteristic:

Items	Symbol	Min	Typ.	Max	Unit	Remark
Operating Luminance	L	136	160	184	Cd/m^2	(1)(5)
Power Consumption	Pon			700	mW	30% pixels on (1)
Response Time	Tres			50	uS	(2)
CIEx (White)	Wx		0.31		-	(5)
CIEy (White)	Wy		0.33		-	(5)
Viewing Angle	VA	160	170		Degree	(3)
Contrast	CR	5000:1	10000:1			(4)
Operation Lifetime	LTop	20000			Hrs	(1)(6)

Note:

Measuring surrounding: dark room

Surrounding temperature: 25°C

1. Test condition:

a. AR_VDD= 4.6V, AR_VSS= -5.4V

b. IC Initial Register Setting:

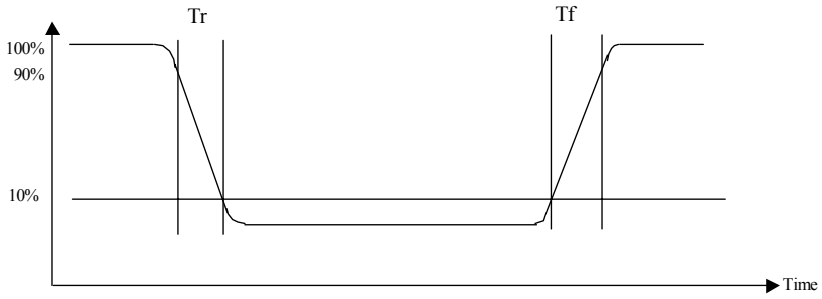
24-bit parallel RGB (DE)
Index_out(0x04); Parameter_out(0x23); //set display mode 24-bit parallel RGB (DE)
Index_out(0x05); Parameter_out(0x82); //set display mode
Index_out(0x07); Parameter_out(0x0F); //set driver capability
Index_out(0x34); Parameter_out(0x18); //set display timing
Index_out(0x35); Parameter_out(0x28); //set display timing
Index_out(0x36); Parameter_out(0x16); //set display timing
Index_out(0x37); Parameter_out(0x01); //set display timing
Index_out(0x02); Parameter_out(0x02); //OTP On
Index_out(0x0A); Parameter_out(0xBB); //VGHVGL=+/-6V
Index_out(0x09); Parameter_out(0x1E); //VGAM1OUT=4.75V
Index_out(0x10); Parameter_out(0x4F); //set R slop
Index_out(0x11); Parameter_out(0x1D); //set G slop
Index_out(0x12); Parameter_out(0x0D); //set B slop
Index_out(0x13); Parameter_out(0x02); //set R_0

Index_out(0x14); Parameter_out(0x07); //set R_10
Index_out(0x15); Parameter_out(0x07); //set R_36
Index_out(0x16); Parameter_out(0x05); //set R_80
Index_out(0x17); Parameter_out(0x04); //set R_124
Index_out(0x18); Parameter_out(0x03); //set R_168
Index_out(0x19); Parameter_out(0x03); //set R_212
Index_out(0x1A); Parameter_out(0x05); //set R_255
Index_out(0x1B); Parameter_out(0x02); //set G_0
Index_out(0x1C); Parameter_out(0x06); //set G_10
Index_out(0x1D); Parameter_out(0x03); //set G_36
Index_out(0x1E); Parameter_out(0x03); //set G_80
Index_out(0x1F); Parameter_out(0x03); //set G_124
Index_out(0x20); Parameter_out(0x03); //set G_168
Index_out(0x21); Parameter_out(0x03); //set G_212
Index_out(0x22); Parameter_out(0x06); //set G_255
Index_out(0x23); Parameter_out(0x02); //set G_0
Index_out(0x24); Parameter_out(0x05); //set B_10
Index_out(0x25); Parameter_out(0x07); //set B_36
Index_out(0x26); Parameter_out(0x05); //set B_80
Index_out(0x27); Parameter_out(0x04); //set B_124
Index_out(0x28); Parameter_out(0x04); //set B_168
Index_out(0x29); Parameter_out(0x04); //set B_212
Index_out(0x2A); Parameter_out(0x05); //set B_255
Index_out(0x06); Parameter_out(0x03); //set display on
AR_VDD= +4.6V
AR_VSS= -5.4V

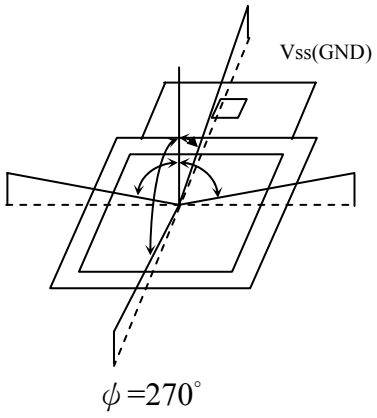
8-bit serial RGB (DE)
Index_out(0x04); Parameter_out(0x21); //set display mode 8-bit serial RGB (DE)
Index_out(0x05); Parameter_out(0x82); //set display mode
Index_out(0x07); Parameter_out(0x0F); //set driver capability
Index_out(0x34); Parameter_out(0x48); //set display timing
Index_out(0x35); Parameter_out(0x78); //set display timing
Index_out(0x36); Parameter_out(0x42); //set display timing
Index_out(0x37); Parameter_out(0x01); //set display timing
Index_out(0x02); Parameter_out(0x02); //OTP On
Index_out(0x0A); Parameter_out(0xBB); //VGHVGL=+/-6V
Index_out(0x09); Parameter_out(0x1E); //VGAM1OUT=4.75V

Index_out(0x10); Parameter_out(0x4F); //set R slop
Index_out(0x11); Parameter_out(0x1D); //set G slop
Index_out(0x12); Parameter_out(0x0D); //set B slop
Index_out(0x13); Parameter_out(0x02); //set R_0
Index_out(0x14); Parameter_out(0x07); //set R_10
Index_out(0x15); Parameter_out(0x07); //set R_36
Index_out(0x16); Parameter_out(0x05); //set R_80
Index_out(0x17); Parameter_out(0x04); //set R_124
Index_out(0x18); Parameter_out(0x03); //set R_168
Index_out(0x19); Parameter_out(0x03); //set R_212
Index_out(0x1A); Parameter_out(0x05); //set R_255
Index_out(0x1B); Parameter_out(0x02); //set G_0
Index_out(0x1C); Parameter_out(0x06); //set G_10
Index_out(0x1D); Parameter_out(0x03); //set G_36
Index_out(0x1E); Parameter_out(0x03); //set G_80
Index_out(0x1F); Parameter_out(0x03); //set G_124
Index_out(0x20); Parameter_out(0x03); //set G_168
Index_out(0x21); Parameter_out(0x03); //set G_212
Index_out(0x22); Parameter_out(0x06); //set G_255
Index_out(0x23); Parameter_out(0x02); //set G_0
Index_out(0x24); Parameter_out(0x05); //set B_10
Index_out(0x25); Parameter_out(0x07); //set B_36
Index_out(0x26); Parameter_out(0x05); //set B_80
Index_out(0x27); Parameter_out(0x04); //set B_124
Index_out(0x28); Parameter_out(0x04); //set B_168
Index_out(0x29); Parameter_out(0x04); //set B_212
Index_out(0x2A); Parameter_out(0x05); //set B_255
Index_out(0x06); Parameter_out(0x03); //set display on
AR_VDD= +4.6V
AR_VSS= -5.4V

2. Response Time test condition



3. Viewing angle test condition:



4. Contrast

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

5. Optical tester: CA210

6. Brightness of 30% power consumption. Operating Life Time is defined when the luminance has decayed to less than 50% of the initial measured luminance before life test.

7. System Diagram:

TBD

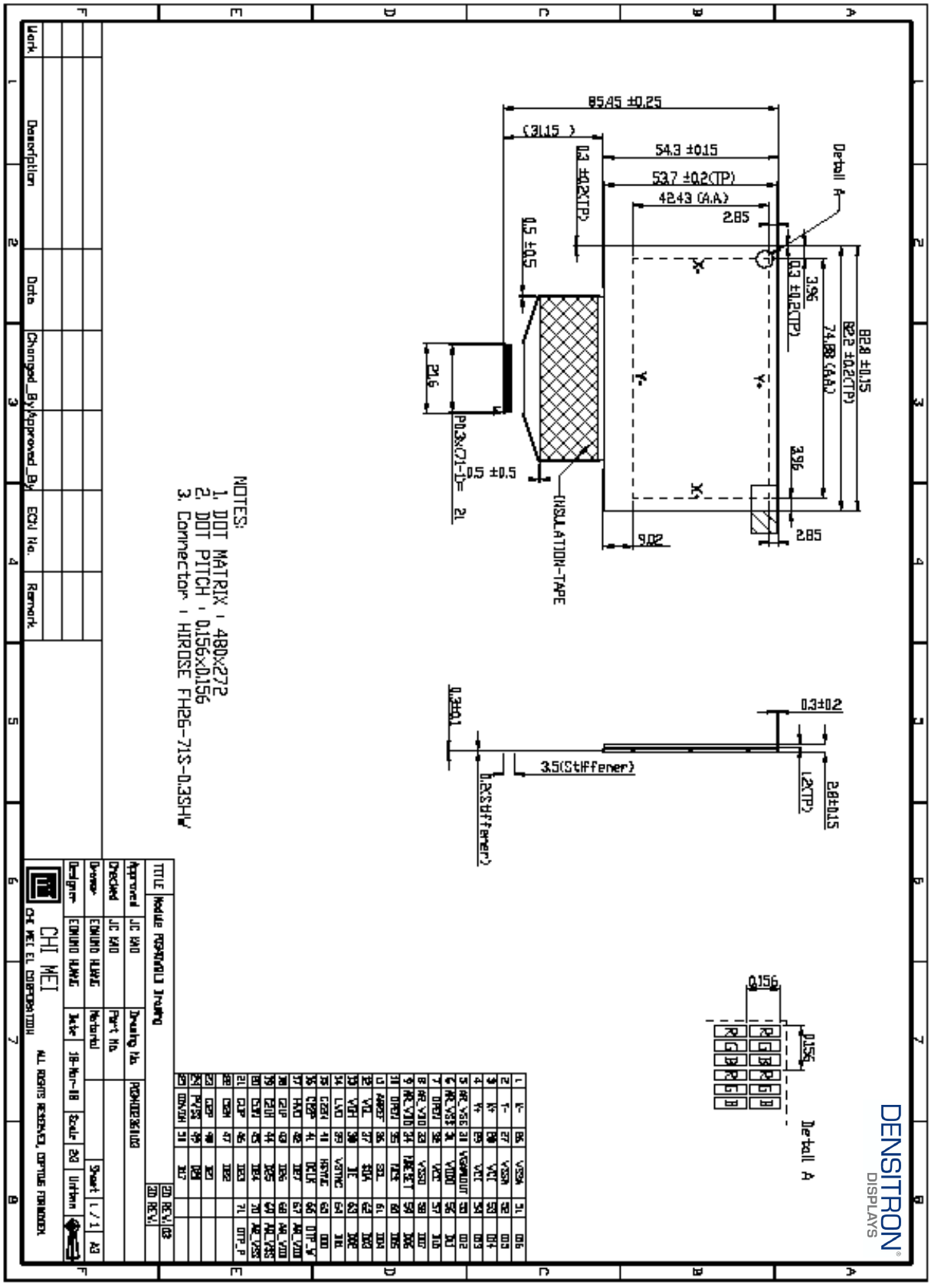
8. Pin Assignment:

PIN	Symbol	I/O	Description	Remarks
1	TP1	I	Touch panel P1	
2	TP2	I	Touch panel P2	
3	TP3	I	Touch panel P3.	
4	TP4	I	Touch panel P4	
5	AR_VSS	I	Negative voltage for OLED	
6	AR_VSS	I	Negative voltage for OLED	
7	TEST1_VS	**open**	**CMEL test pin, it must be open.**	
8	AR_VDD	I	Positive voltage for OLED	
9	AR_VDD	I	Positive voltage for OLED	
10	TEST2_VD	**open**	**CMEL test pin, it must be open.**	
11	ARREF	I/O	Panel refers voltage of the regulator ARREF or external input voltage. (-8V~+8V)	
12	VGL	I/O	Low Voltage output of regulator VGL or external input voltage. (-3V~-8V)	
13	VGH	I/O	High Voltage output of regulator VGH or external input voltage. (+3V~+8V)	
14	LVO	I/O	**Negative output voltage of the booster2. (-8.5V)**	
15	C22N	I/O	Connect to the step-up circuit, capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.	
16	C22P			
17	HVO	I/O	Positive output voltage of the booster2. (8.5V)	
18	C21P	I/O	Connect to the step-up circuit, capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.	
19	C21N			
20	C11N	I/O	Connect to the step-up circuit, 4capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.	
21	C11P			
22	C12N			
23	C12P			
24	PVSS	P	Charge pump ground pin, it must connect to external ground.	
25	DDVDH	I/O	Output voltage of the booster1. (5.1V/6.0V)	
26	VSSA	P	**Analog ground pin. It must connect to external ground.**	
27	VSSA	P	**Analog ground pin. It must connect to external ground.**	
28	VCI	P	**A power supply for the Analog circuit. (2.7V~3.6V)**	
29	VCI	P	**A power supply for the Analog circuit. (2.7V~3.6V)**	
30	VGAM1OUT	I/O	Output voltage of the VGAM1OUT regulator and used positive power of source driver. (4.8V/5.8V)	
31	VDDD	I/O	Internal logic voltage input or output pin VDC_ENB=0, VDDD is output, please connect to 1uF capacitor. VDC0 / VDDD / Status 0 / 1.8V / Normal display	

			1 | 2.5V | OTP program **VDC_ENB=1, VDDD is input. (Input range = 1.6V~2.75V)**	
32	VCC	P	**A power supply for the Digital circuit. (1.5V~3.6V)**	
33	VSSD	P	**Digital ground pin. It must connect to external ground.**	
34	NRESET	I	**Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.** (Normally pull high)	
35	NCS	I	**Serial Interface chip enable pin.** (Normally pull high)	
36	SCL	I	**Serial Interface clock input pin.** (Normally pull high)	
37	SDA	I	**Serial Interface data line.** (Normally pull high)	
38	DE	I	Data enable: When VSYNC+HSYNC+DE mode, DE=H: Data enable, DE=L: Data disable (Black). **(Normally pull low)**	
39	VSYNC	I	Frame synchronizing signal. If VSPL=0: Active low. If VSPL=1: Active high.	
40	HSYNC	I	Line synchronizing signal. If HSPL=0: Active low. **If HSPL=1: Active high.**	
41	DCLK	I	Dot clock signal. If DPL=0: Data are input on the rising edge of DOTCLK. **If DPL=1: Data are input on the falling edge of DOTCLK.**	
42	D27	I	Digital data input. DX0 is LSB and DX7 is MSB. **(Normally pull low)** 1. If parallel RGB input mode is used, D0X, D1X, and D2X indicate R, G, and B data in turn. 2. If serial RGB or RGBD or CCIR601 or CCIR656 input mode is selected, only D07~D00 are used, and others short to GND. **DX7~DX0 has 8-bit width, respectively to compose 16,777,216 color and 256 gray scale of 1 pixel.**	
43	D26			
44	D25			
45	D24			
46	D23			
47	D22			
48	D21			
49	D20			
50	D17			
51	D16			
52	D15			
53	D14			
54	D13			
55	D12			
56	D11			
57	D10			
58	D07			
59	D06			

60	D05			
61	D04			
62	D03			
63	D02			
64	D01			
65	D00			
66	**TEST3_W**	**open**	**CMEL test pin, it must be open.**	
67	**AR_VDD**	I	Positive voltage for OLED	
68	**AR_VDD**	I	Positive voltage for OLED	
69	**AR_VSS**	I	Negative voltage for OLED	
70	**AR_VSS**	I	Negative voltage for OLED	
71	**TEST4_P**	**open**	**CMEL test pin, it must be open.**	

9. External Dimension:



10. Reliability Test:

TBD

11. Package:

TBD